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# SURVEY REPORT FOR SPLIT RADIX FFT ALGORITHM

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**Abstract:**

Fast Fourier Transform (FFT) processor is one of the important key procedures in Orthogonal Frequency Division Multiplexing (OFDM) communication systems. Split-radix Fast Fourier Transform (SRFFT) approximates the minimum number of multiplications compared to other FFT algorithm; therefore SRFFT is good for the implementation of low power FFT processor**.** This proposed paper discussion various techniques proposed earlier in the literature for reduction of power consumption. Comparative study of various FFT algorithm proposed by researches for power reduction.

**Key Words:** Fast Fourier Transform (FFT) & Split Radix FFT (SRFFT).

## 1. Introduction:

For orthogonal frequency division multiplexing (OFDM) applications, the FFT is performed with algorithms of signal processing. FFT Architecture with Delay Feedback (DF) and Delay Commutator (DC) structure is used to realise frequency transformations. In this section, Radix-2 Single Delay Feedback (R2SDF)-Radix-4 Multiple Delay Commutator (R4MDC) FFT architecture and their performances are analyzed. The proposed FFT architecture is used to determine the frequency representation of discrete time input sampled signals. Performance of twiddle factor multiplication is improved by introducing Bit Parallel Multiplier (BPM). Bit Parallel Multiplier (BPM) structure is also used to reduce the hardware utilization. Proposed Mixed R2SDF-R4MDC FFT Architecture is generating the better ADP (Area Delay Power) Product in terms of VLSI Concerns. To improve the performance of FFT Processor, R2SDF-R4MDC FFT Architecture with low computational path is proposed in this section. Fast Fourier Transformation (FFT) is play as a important role in Orthogonal Frequency Division Multiplexing (OFDM) applications.. There are two architectures is used in FFT that is Memory based architecture, Pipelined architecture. Pipelined architecture is mainly used to compute the FFT Algorithm. For power optimizations, the Split radix multipath delay commutator (SRMDC) FFT Architecture is implemented. Split radix algorithm is varied the various number of butterfly stages in successful stages to determine the frequency transformation. In general, the architecture performed with single stage single path delay feedback (SDF). Single Delay Feedback (SDF) and Multiple Delay Commutator (MDC) have separate advantage and disadvantage itself due to this functionality. To achieve the both advantages within one architecture, the combined SDF-MDC Architecture based Split radix FFT Computations are achieved in this research work. In general, single Delay Feedback (SDF) is suitable for high speed applications and Multipath Delay Commutator (MDC) is suitable for low power applications. Split Radix algorithm is based on the concepts for both Radix-2 and Radix-4 FFT Algorithm. In Radix-4 algorithm, the even points of the samples are computed and split radix algorithms compute the even points of the samples.

## 2. Literature Review:

Kannaiah R et al., [1] presented the combined Radix-4 SDC-SDF FFT Architecture for I/O Pipelined. To reduce the hardware utilization, the Radix-2 Single Delay Commutator (SDC) FFT Architecture is proposed by sharing the common arithmetical operations. In that case, the hardware utilization is achieved but the requirement of arithmetical operation is high. To reduce the arithmetical operations such as adders and multipliers, the Combined SDC-SDF FFT Architecture is proposed. Multiple Delay Commutator (MDC) FFT architecture is the direct implementation approach with 50% of hardware utilization. Single Delay Feedback (SDF) and Single Delay Commutator (SDC) is required less number of memory elements. The combined SDF-SDC FFT Architecture is mainly used to reduce the arithmetical operations such as adders and multipliers with normal order input and output sequence.

Banothu Dharma et al., [2] described the Radix-4 FFT Architecture based on CSD Algorithm. The new Canonic signed digit (CSD) algorithm based FFT Architecture is used to reduce the computational path. Requirement of addition function is equal to the one less than the number of non zero bits in constant multiplication method. For area and power consumptions, the conventional multiplier digit is replaced by the signed digit code. Common sub expression sharing approach is used to reduce the hardware utilization as well as requirement of adders and shifters. That approach is mainly used for filter like operations. Multiplication process is one of the complicate process, to design a multiplier less FFT the Radix-4 Single delay commutator (SDC) FFT architecture is designed. In that architecture it has only add/shift functional units. This architecture generates the efficient power optimization than the conventional multiplier based FFT architecture.

Manimaran et al., [3] stated the pipelined Radix-4 Single path-Delay commutator (SDC) FFT architecture. Delay Feedback (DF) and Delay Commutator (DC) are the types of pipelined architectures with their properties such as small chip area, high throughput and low power. The memory utilization (N-1) is highly

achieved in SDF FFT Architecture but the requirement of butterfly element is not efficiently achieved. Processing elements, Commutator and delay is the elements of commutator architecture. Processing element is used to perform the addition and subtraction function and commutator is used to convert the signal from one form into another. Reduction of adder and shifter is achieved by the twiddle factor. The signal is controlled by the multiplexer. The proposed Radix-4 Single Delay Commutator (SDC) FFT architecture is reduced the hardware usage as well as power consumptions with modifications of butterfly elements. This SDC architecture also performed with less number of computational paths than SDF FFT.

Angeline T et al., [4] explained the Fast Fourier Transform (FFT) Processors. Divide & Conquer and Recursion is the two methods in FFT Processors. By using those methods, the algorithm is explained in FFT. FFT has several architectures itself such as, Single memory, Dual memory, Array memory, Cached memory and Pipelined architectures. For real time applications, the FFT Architecture is designed by using pipelined architecture with high throughput. Pipeline architecture is classified based on path (Single path and multiple path). Delay feedback (DF) and Delay commutator (DC) is used for frequency transformations. Radix-2 Single path delay feedback (SDF) and Radix-4 Single path delay commutator is the types of Single path architectures. Radix-4 Multiple path Delay Commutator (MDC), Mixed radix Multiple path Delay Commutator (MRMDC) and Split radix multiple path delay commutator (SRMDC) is the types of multiple path architectures. Single path architecture is provide memory utilizations and hardware utilizations but its has less throughput. To generate high throughput, the multiple path architecture is designed. Memory utilization is not achieved in multiple path architecture.

Srikanth P K et al., [5] described 64 point FFT Architecture with pipelined architecture. For both low power consumption and high speed applications, the pipelined FFT architecture is highly suitable to perform. In existing architectures, the read only memory (ROMs) is used to store the twiddle factors for multiplication process. Reconfigurable complex multiplier and bit parallel multiplier based FFT architecture is proposed to eliminate the ROMs and utilize the less amount of power. In proposed FFT architecture, the Complex multiplier and Bit parallel multiplier is used instead of memory elements (ROMs). To achieve efficient Area Delay Product (ADP) the utilizations of memory elements is eliminated in FFT Processor.

Sowjanya K et al., [6] explained the performance analysis of FFT algorithm using multiple radix algorithms. By combining two or more various radices computational path of the FFT is a result a split radix algorithm. In split radix algorithm, the computational point is separated into two components that are odd and even. That even components are dissolved into 8n and odd components are dissolved into 4n+1 respectively. The FFT Algorithm is designed by various design methodologies (Radix-2, Radix-8, Split radix) to evaluate the performance analysis. The less number of LUT utilizations and delay is considering for the efficient design of FFT Algorithm.

Harpreet Kaur et al., [7] described the FPGA Implementation of the mixed radix algorithm. Decimation in time (DIT) domain based FFT by using mixed radix is mainly focused in this work for digital communications. Radix-4 and Radix-2 algorithm has several advantages in terms of Area, Delay and power. In Radix-8 algorithm, the twiddle factor is multiplied with the samples and it's indicated by the number of overflow lines. Since N=4*8, the number of computational stages are reduced by the 2. i.e. N=2 Stages. In Radix-4 algorithm, the computational advantage is better than the radix-2 algorithm because the working of four Radix-2 butterflies is compensated by the one Radix-4 butterfly and also the requirement of the complex multiplier is less than the Radix-2 algorithm. The mixed radix FFT algorithm is generating the efficient ADP product and this FFT Algorithm is implemented in the Spartan-6 FPGA to evaluate the performance analysis.

Asmita Haveliya., [8] stated the 32 point Radix-2 algorithm for FPGA implementation. In general, the $N^2$ complex multiplications required to compute the all N values. There are four real multiplications and two real additions required to perform complex multiplications and two real additions required for complex addition process. These make high number of computational path. Decimation in time (DIT) FFT algorithm is separated into the odd and even samples. To reduce the entire computational cost, the various outputs are generated by the reuse of minimum FFT outputs. These FFT design is applicable for hardware implementations with Vertex FPGA.

**3. Future Enhancement and Conclusion:**

FFT (Fast Fourier Transform) architecture performs with high memory and multiplier utilizations. By decompose the radix-8 FFTs, the 64-Point FFT design is evaluated. Decompositions lead to the reductions of the twiddle factors and also reduce the requirement of the complex multiplier. Modified booth multiplication is used for the complex multiplications of twiddle factor. Controller, Radix-4 (stage 1 & stage 3), Radix-2 (stage 2 & stage 4) and Trivial, Nontrivial twiddle factor are functional elements of the design architecture. To order the data from serial to serial, the reorder stage is used in integral stage of the design. By using VHDL language, the design is verified and simulated. Proposed design is performs with the low area, efficient power consumptions and latency in terms of VLSI Concerns.

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